DDR3L SDRAM
ECC SO-DIMMs
Based on 4Gb B-die

HMT451A7BFR8A
HMT41GA7BFR8A

*SK hynix reserves the right to change products or specifications without notice.

Revision History

Revision No.	History	Draft Date	Remark
1.0	Initial Release	Oct. 2014	

Description

SK hynix 204pin ECC-SO-UDIMMs (72bit-wide, Double Data Rate Synchronous DRAM Small Outline Dual In-Line Memory Modules) are low power, high-speed operation memory modules. These ECC-SD-UDIMMs are intended for use as computing memory when installed in systems such as embedded systems and servers, workstations.ECC-SO-DIMMs are running at 533/667/800 MHz clock speed and offering. 8500/ 10600/12800/14900 MB/s bandwidth on the primary data bus.

Features

- Power Supply: VDD=1.35V (1.283V to 1.45V)
- VDDQ = 1.35V (1.283V to 1.45V)
- VDDSPD=3.0V to 3.6V
- Backward Compatible with 1.5V DDR3 Memory module
- 8 internal banks
- Data transfer rates: PC3-14900, PC3-12800, PC3-10600, PC3-8500
- Bi-directional Differential Data Strobe
- 8 bit pre-fetch
- Burst Length (BL) switch on-the-fly: BL 8 or BC (Burst Chop) 4
- On Die Termination (ODT) supported
- This product is in compliance with the RoHS directive.

Ordering Information

Part Number	Density	Organization	Component Composition	# of ranks
HMT451A7BFR8A-G7/H9/PB/RD	4GB	512Mx72	512Mx8(H5TC4G83BFR)*9	1
HMT41GA7BFR8A-G7/H9/PB/RD	8GB	1Gx72	512Mx8(H5TC4G83BFR)*18	2

Key Parameters

MT/s	Grade	tCK (ns)	CAS Latency (tCK)	tRCD (ns)	tRP (ns)	tRAS (ns)	tRC (ns)	CL-tRCD-tRP
DDR3L-1066	-G7	1.875	7	13.125	13.125	37.5	50.625	7-7-7
DDR3L-1333	-H9	1.5	9	13.5 (13.125)*	13.5 (13.125)*	36	49.5 (49.125)*	9-9-9
DDR3L-1600	-PB	1.25	11	13.75 (13.125)*	13.75 (13.125)*	35	48.75 (48.125)*	11-11-11
DDR3L-1866	-RD	1.07	13	13.91 (13.125)*	13.91 (13.125)*	34	47.91 (47.125)*	13-13-13

*SK hynix DRAM devices support optional downbinning to CL11, CL9 and CL7. SPD setting is programmed to match.

Speed Grade

Grade	Frequency [Mbps]									Remark
	CL5	CL6	CL7	CL8	CL9	CL10	CL11	CL12	CL13	
-G7	667	800	1066	1066						
-H9	667	800	1066	1066	1333	1333				
-PB	667	800	1066	1066	1333	1333	1600			
-RD		800	1066	1066	1333	1333	1600		1866	

Address Table

	4GB(1Rx8)	8GB(2Rx8)
Refresh Method	8K/64ms	8K/64ms
Row Address	A0-A15	A0-A15
Column Address	A0-A9	A0-A9
Bank Address	BA0-BA2	BA0-BA2
Page Size	1KB	1KB

Pin Descriptions

Pin Name	Description	Number	Pin Name	Description	Number
CK0	Clock Input, positive line	1	ODT[1:0]	On Die Termination Inputs	2
$\overline{CK0}$	Clock Input, negative line	1	DQ[63:0]	Data Input/Output	64
CK1	Clock Input, positive line	1	CB[7:0]	Data check bits Input/Output	8
$\overline{CK1}$	Clock Input, negative line	1	DQS[8:0]	Data strobes	9
CKE[1:0]	Clock Enables	2	$\overline{DQS}$[8:0]	Data strobes, negative line	9
$\overline{RAS}$	Row Address Strobe	1	DM[8:0]	Data Masks	9
$\overline{CAS}$	Column Address Strobe	1			
$\overline{WE}$	Write Enable	1			
$\overline{S}$[3:0]	Chip Selects	4	$\overline{EVENT}$	Reserved for optional hardware temperature event pin	1
A[9:0],A11, A[15:13]	Address Inputs	14			
A10/AP	Address Input/Autoprecharge	1	$\overline{RESET}$	Reset and SDRAM control pin	1
A12/$\overline{BC}$	Address Input/Burst chop	1	V_{DD}	Power Supply	xx
BA[2:0]	SDRAM Bank Addresses	3	V_{SS}	Ground	xx
SCL	Serial Presence Detect (SPD) Clock Input	1	V_{REFDQ}	Reference Voltage for DQ	1
SDA	SPD Data Input/Output	1	V_{REFCA}	Reference Voltage for CA	1
SA[1:0]	SPD Address Inputs	2	V_{TT}	Termination Voltage	2
Par_In	Parity bit for the Address and Control bus	1	V_{DDSPD}	SPD Power	1
$\overline{Err\_Out}$	Parity error found on the Address and Control bus	1		**Total : 204**	

Input/Output Functional Descriptions

Symbol	Type	Polarity	Function
CK0	IN	Positive Edge	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM Clock Driver (72b-SO-RDIMM), on-DIMM PLL (72b-SO-CDIMM), or to DRAM on rank 0 (72b-SD-DIMM).
$\overline{CK0}$	IN	Negative Edge	Negative line of the differential pair of system clock inputs that drives input to the on-DIMM Clock Driver (72b-SO-RDIMM), on-DIMM PLL (72b-SO-CDIMM), or to DRAM on rank 0 (72b-SD-DIMM).
CK1	IN	Positive Edge	Positive line of a secondary differential pair of system clock inputs. Teminated but not used on 72b-SO-RDIMMs or 72b-SO-CDIMMs. Connected to DRAMs on rank 1 or 72b-SD-DIMMs.
CK0/$\overline{CK0}$ CK1/$\overline{CK1}$	IN	Negative Edge	Negative line of a secondary differential pair of system clock inputs. Teminated but not used on 72b-SO-RDIMMs or 72b-SO-CDIMMs. Connected to DRAMs on rank 1 or 72b-SD-DIMMs.
CKE[1:0]	IN	Active High	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provieds PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). Connected to the registering clock driver on 72b-SO-RDIMMs, connected to DRAMs on 72b-SO-CDIMMs and 72b-SO-DIMMs.
$\overline{S[1:0]}$	IN	Active Low	Enables the command decoders for the associated rank of SDRAM when low and disables decoders when high. When decoders are disabled, new commands are ignored and previous operations continue. Connected to SDRAMs on 72b-SD-CDIMMs and 72b-SO-DIMMs. For 72b-SO-RDIMMs, the combinations of these input signals perform unique functions, including disabling all outputs (except CKE and ODT) of the register(s) on the DIMM or accessing internal control words in the register device(s). For modules with two registers, S[3:2] operate similarly to S[1:0] for the second set of register outputs or register control words.
ODT[1:0]	IN	Active High	On-Die Termination control signals. Connected to SDRAMs on 72b-SO-CDIMMs and 72b-SO-DIMMs, connected to the registering clock driver on 72b-SO-RDIMMs.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	IN	Active Low	When sampled at the positive rising edge of the clock. $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM. Connected to SDRAMs on 72b-SO-CDIMMs and 72b-SO-DIMMs, connected to the registering clock driver on 72b-SO-RDIMMs.
V_{REFDQ}	Supply		Reference voltage for DQ0-DQ63 and CB0-CB7.
V_{REFCA}	Supply		Reference voltage for A0-A15, BA0-BA2, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{S0}$, $\overline{S1}$, CKE0, CKE1, Par_In, ODT0 and ODT1.
BA[2:0]	IN	—	Selects which SDRAM internal bank of eight is activated. BA0 - BA2 define to which bank an Active, Read, Write or Precharge commnad is being applied. Bank address also derermines mode register is to be accessed during an MRS cycle. Connected to SDRAMs on 72b-SO-CDIMMs and 72b-SO-DIMMs, connected to the registering clock driver on 72b-SO-RDIMMs.
A[9:0], A10/AP, A11, A12/$\overline{BC}$ A[15:13]	IN	—	Provided the row address for Active commnads and the column address and Auto Precharge bit for Read/Write commands to select one lacation out of the memory array in the respective bank. A10 is sampled during a Precharge command to detemine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also utilized for BL 4/8 identification for “BL on the fly” during CAS command. The address inputs also provied the op-code during Mode Register Set commands. Connected to SDRAMs on 72b-SO-CDIMMs and 72b-SO-DIMMs, connected to the registering clock driver on 72b-SO-RDIMMs.

Symbol	Type	Polarity	Function
DQ[63:0] CB[7:0]	I/O	—	Data and Check Input/Output pins.
DM[8:0]	IN	Active High	Mask write data when high, issued concurrently with input data.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR3 SDRAM input buffers and core logic.
V_{TT}	Supply		Termination Voltage for Address/Command/Control/Clock nets.
DQS1[7:0]	I/O	Positive Edge	Positive line of the differential data strobe for input and output data
$\overline{DQS[7:0]}$, $\overline{DQS[7:0]}$	I/O	Negative Edge	Negative line of the differential data strobe for input and output data
SA[1:0]	IN	—	These signals are tied at the system planar to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA	I/O	—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pullup.
SCL	IN	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DDSPD} on the system planar to act as a pullup.
$\overline{EVENT}$	OUT (open drain)	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device.The system should guarantee the electrical level requirement is met for the $\overline{EVENT}$ pin on TS/SPD part.
V_{DDSPD}	Supply		Serial EEPROM positive power supply wired to a separate power pin at the connector which supports from 3.0 Volt to 3.6 Volt (nominal 3.3V) operation.
RESET	IN		The RESET pin is connected to the RESET pin on the register (72b-SD-RDIMM) and to the RESET pin on the SDRAMs (all modules). When low, all register outputs will be driven low and the Clock Driver clocks to the DRAMs and register(s) will be set to low lever (the Clock Driver will remain synchronized with the input clock).
Par_in	IN		Parity bit for the Address and Control bus. (“1”: Odd, “0”: Even). Not used on 72b-SO-DIMMs or 72b-SO-CDIMMs.
$\overline{Err\_Out}$	OUT (open drain)		Parity error detected on the Address and Control bus. A resistor may be connected from $\overline{Err\_Out}$ bus line to V on the system planner to act as a pull up. Not used on 72b-SO-DIMMs or 72b-SO-CDIMMs.

Pin Assignments

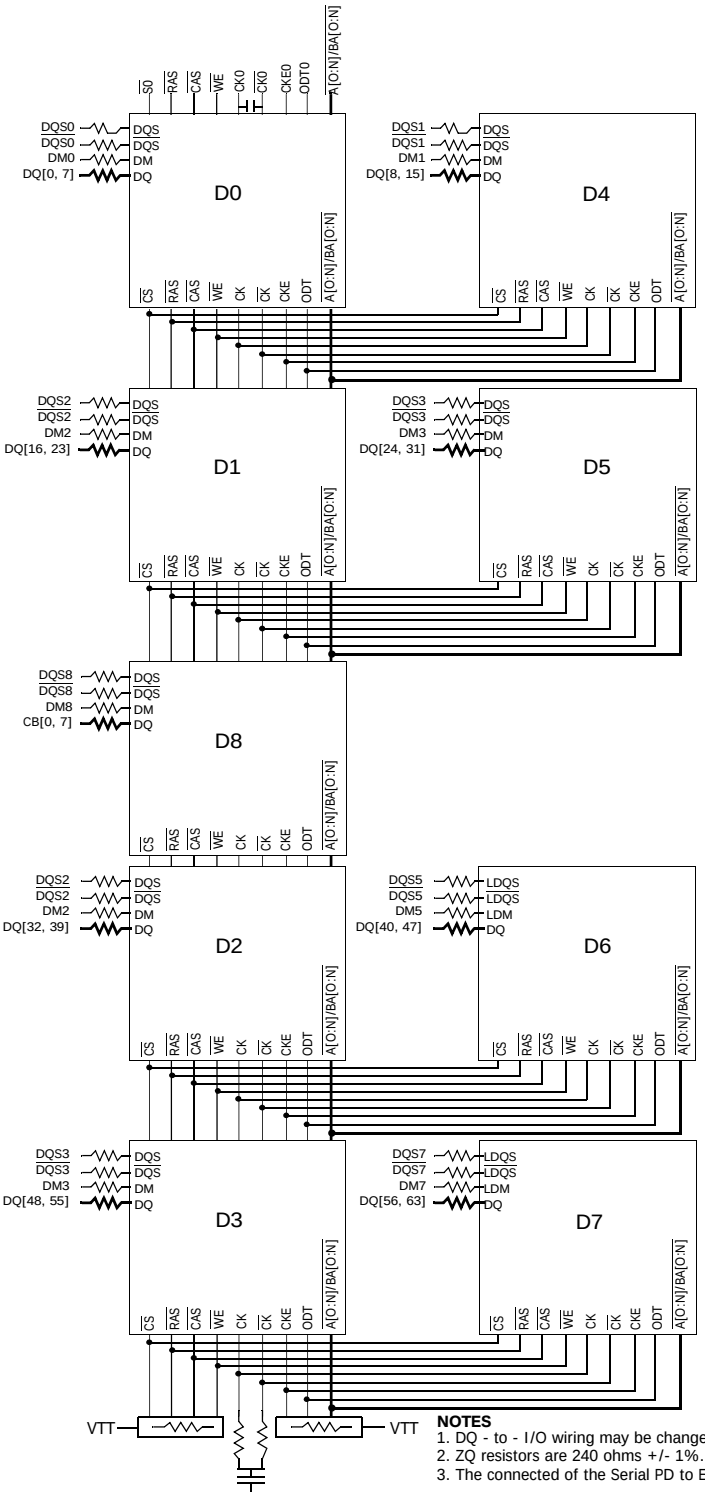
Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	$V_{REF}DQ$	2	V_{SS}	53	V_{SS}	54	DQ28	103	A3	104	A4	155	V_{SS}	156	DQS5
3	V_{SS}	4	DQ4	55	DQ24	56	DQ29	105	A1	106	A2	157	DM5	158	V_{SS}
5	DQ0	6	DQ5	57	DQ25	58	V_{SS}	107	A0	108	BA1	159	DQ42	160	DQ46
7	DQ1	8	V_{SS}	59	DM3	60	$\overline{DQS3}$	109	V_{DD}	110	V_{DD}	161	DQ43	162	DQ47
9	V_{SS}	10	$\overline{DQS0}$	61	V_{SS}	62	DQS3	111	CK0	112	$\overline{Par\_In}$, NC, CK1	163	V_{SS}	164	V_{SS}
11	DM0	12	DQS0	63	DQ26	64	V_{SS}	113	$\overline{CK0}$	114	$\overline{Err\_Out}$, NC, CK1	165	DQ48	166	DQ52
13	DQ2	14	V_{SS}	65	DQ27	66	DQ30	115	V_{DD}	116	V_{DD}	167	DQ49	168	DQ53
15	DQ3	16	DQ6	67	V_{SS}	68	DQ31	117	A10/AP	118	$\overline{S3}$	169	V_{SS}	170	V_{SS}
17	V_{SS}	18	DQ7	69	CB0	70	V_{SS}	119	BA0	120	$\overline{S2}$	171	$\overline{DQS6}$	172	DM6
19	DQ8	20	V_{SS}	71	CB1	72	CB4	121	$\overline{WE}$	122	$\overline{RAS}$	173	DQS6	174	DQ54
21	DQ9	22	DQ12	Key				123	V_{DD}	124	V_{DD}	175	V_{SS}	176	DQ55
23	V_{SS}	24	DQ13	73	V_{SS}	74	CB5	125	$\overline{CAS}$	126	ODT0	177	DQ50	178	V_{SS}
25	$\overline{DQS1}$	26	V_{SS}	75	$\overline{DQS8}$	76	DM8	127	$\overline{S0}$	128	ODT1	179	DQ51	180	DQ60
27	DQS1	28	DM1	77	DQS8	78	V_{SS}	129	$\overline{S1}$	130	A13	181	V_{SS}	182	DQ61
29	V_{SS}	30	$\overline{RESET}$	79	V_{SS}	80	CB6	131	V_{DD}	132	V_{DD}	183	DQ56	184	V_{SS}
31	DQ10	32	V_{SS}	81	CB2	82	CB7	133	DQ32	134	DQ36	185	DQ57	186	$\overline{DQS7}$
33	DQ11	34	DQ14	83	CB3	84	$V_{REF}CA$	135	DQ33	136	DQ37	187	V_{SS}	188	DQS7
35	V_{SS}	36	DQ15	85	V_{DD}	86	V_{DD}	137	V_{SS}	138	V_{SS}	189	DM7	190	V_{SS}
37	DQ16	38	V_{SS}	87	CKE0	88	A15	139	$\overline{DQS4}$	140	DM4	191	DQ58	192	DQ62
39	DQ17	40	DQ20	89	CKE1	90	A14	141	DQS4	142	DQ38	193	DQ59	194	DQ63
41	V_{SS}	42	DQ21	91	BA2	92	A9	143	V_{SS}	144	DQ39	195	V_{SS}	196	V_{SS}
43	$\overline{DQS2}$	44	DM2	93	V_{DD}	94	V_{DD}	145	DQ34	146	V_{SS}	197	SA0	198	$\overline{EVENT}$
45	DQS2	46	V_{SS}	95	A12/$\overline{BC}$	96	A11	147	DQ35	148	DQ44	199	VDD_{SPD}	200	SDA
47	V_{SS}	48	DQ22	97	A8	98	A7	149	V_{SS}	150	DQ45	201	SA1	202	SCL
49	DQ18	50	DQ23	99	A5	100	A6	151	DQ40	152	V_{SS}	203	V_{TT}	204	V_{TT}
51	DQ19	52	V_{SS}	101	V_{DD}	102	V_{DD}	153	DQ41	154	$\overline{DQS5}$				

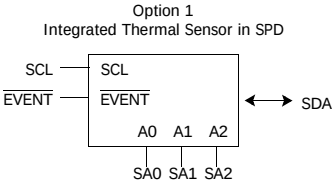
NC = No Connect

Notes on following page for differences of 72b-SO-RDIMMs, 72b-SO-CDIMMs, 72b-SO-DIMMs

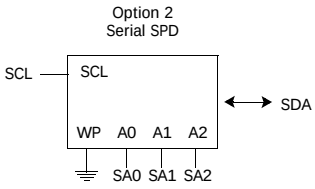
Functional Block Diagram

4GB, 51Mx72 Module(1Rank of x8)

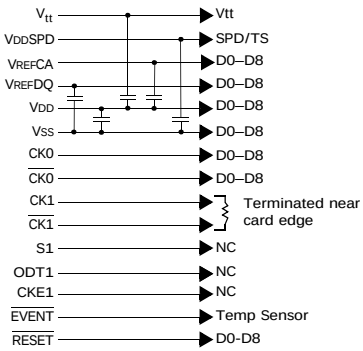




Sensor PD w/Integrated Thermal Sensor



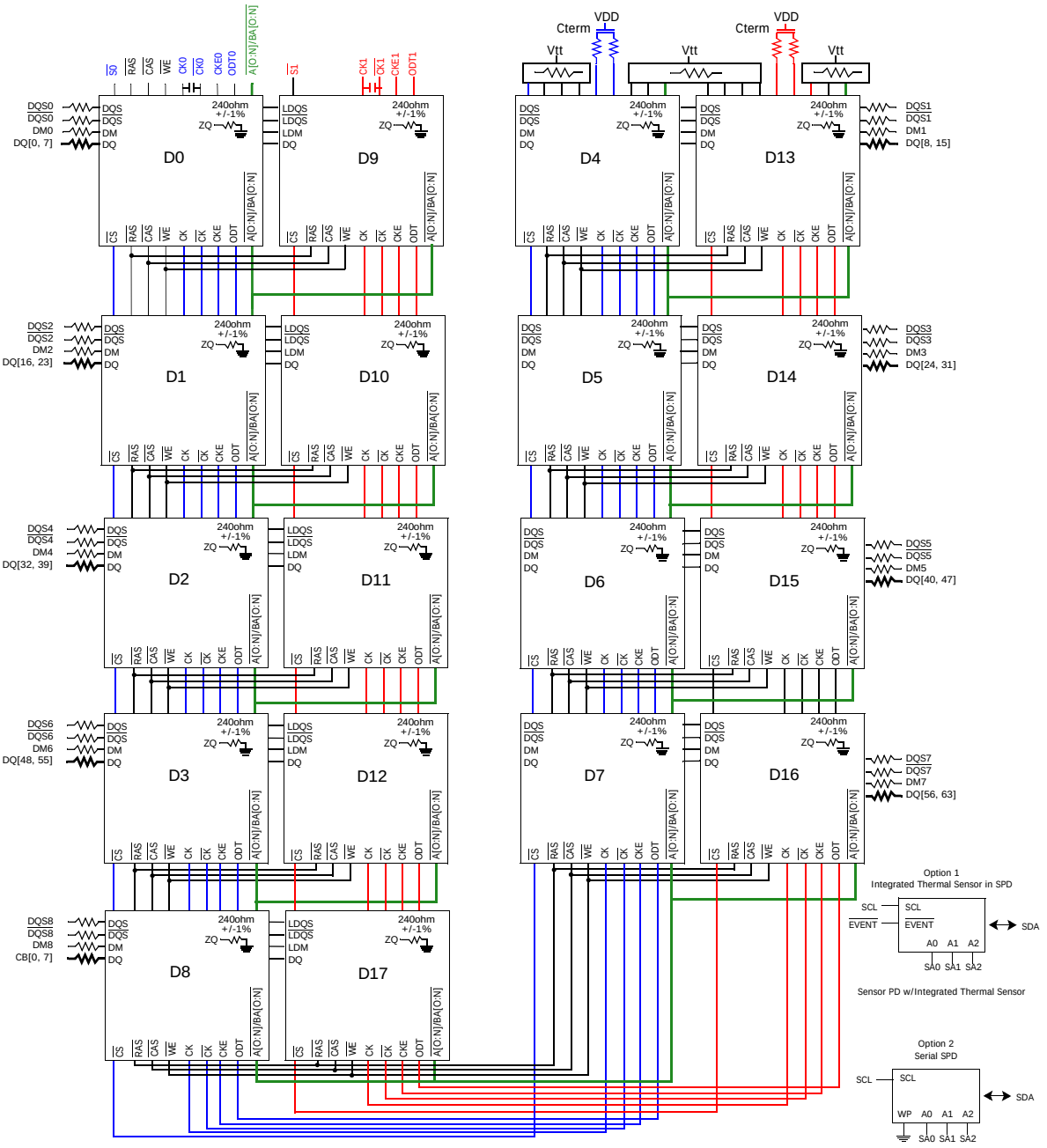
Sensor PD no Thermal Sensor



NOTES

1. DQ - to - I/O wiring may be changed within a byte
2. ZQ resistors are 240 ohms +/- 1%. For all other resistor values refer to the appropriate wiring diagram.
3. The connected of the Serial PD to EVENT (option 1) or to ground (option 2) is realized by resistor options.

8GB, 1Gx72 Module(2Rank of x8)



NOTES

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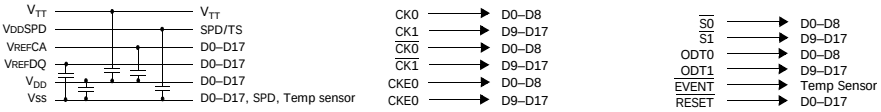
2. ZQ resistors are 240 ohms +/- 1%. For all other resistor values refer to the appropriate wiring diagram.
3. The connected of the Serial PD to EVENT (option 1) or to ground (option 2) is realized by resistor options.



Absolute Maximum Ratings

Absolute Maximum DC Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 0.4 V ~ 1.80 V	V	1,
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.4 V ~ 1.80 V	V	1,
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	- 0.4 V ~ 1.80 V	V	1
T_{STG}	Storage Temperature	-55 to +100	^{o}C	1, 2

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6XVDDQ,When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

DRAM Component Operating Temperature Range

Temperature Range

Symbol	Parameter	Rating	Units	Notes
T_{OPER}	Normal Operating Temperature Range	0 to 85	^{o}C	1,2
	Extended Temperature Range	85 to 95	^{o}C	1,3

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85^{o}C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85^{o}C and 95^{o}C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a. Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability
   b. If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b). DDR3 SDRAMs support Extended Temperature Range and please refer to component datasheet and/or the DIMM SPD for tFEFI requirements in the Extended Temperature Range.

AC & DC Operating Conditions

Recommended DC Operating Conditions

Recommended DC Operating Conditions - DDR3L (1.35V) operation

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.283	1.35	1.45	V	1,2,3,4
VDDQ	Supply Voltage for Output	1.283	1.35	1.45	V	1,2,3,4

Notes:

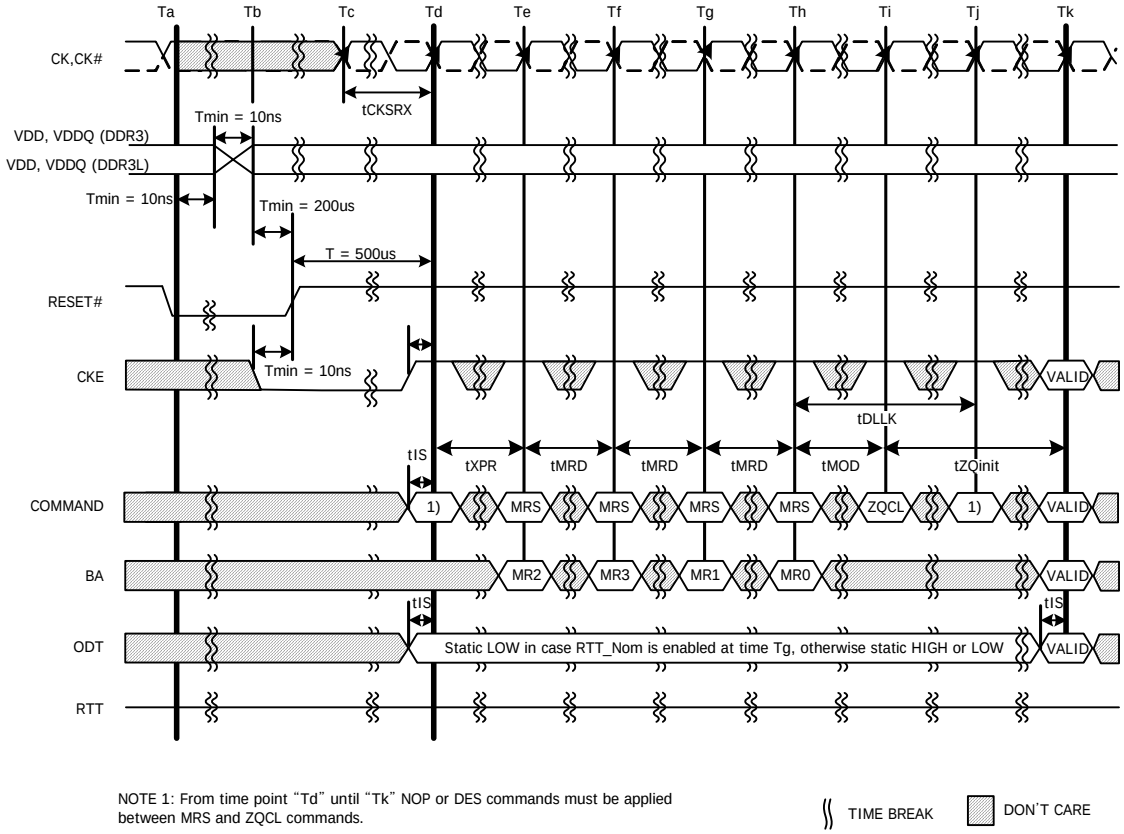
1. Maximum DC value may not be greater than 1.425V. The DC value is the linear average of VDD/VDDQ (t) over a very long period of time (e.g., 1 sec).
2. If maximum limit is exceeded, input levels shall be governed by DDR3 specifications.
3. Under these supply voltages, the device operates to this DDR3L specification.
4. Once initialized for DDR3L operation, DDR3 operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3 operation (see Figure 0).

Recommended DC Operating Conditions - - DDR3 (1.5V) operation

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.5	1.575	V	1,2,3
VDDQ	Supply Voltage for Output	1.425	1.5	1.575	V	1,2,3

Notes:

1. If minimum limit is exceeded, input levels shall be governed by DDR3L specifications.
2. Under 1.5V operation, this DDR3L device operates to the DDR3 specifications under the same speed timings as defined for this device.
3. Once initialized for DDR3 operation, DDR3L operation may only be used if the device is in reset while VDD and VDDQ are changed for DDR3L operation (see Figure 0).



NOTE 1: From time point "Td" until "Tk" NOP or DES commands must be applied between MRS and ZQCL commands.

TIME BREAK DON'T CARE

Figure 0 - VDD/VDDQ Voltage Switch Between DDR3L and DDR3

AC & DC Input Measurement Levels

AC and DC Logic Input Levels for Single-Ended Signals

AC and DC Input Levels for Single-Ended Command and Address Signals

Single Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3L-800/1066		DDR3L-1333/1600		DDR3L-1866		Unit	Notes
		Min	Max	Min	Max	Min	Max		
VIH.CA(DC90)	DC input logic high	Vref + 0.09	VDD	Vref + 0.09	VDD	Vref + 0.09	VDD	V	1
VIL.CA(DC90)	DC input logic low	VSS	Vref - 0.09	VSS	Vref - 0.09	VSS	Vref - 0.09	V	1
VIH.CA(AC160)	AC input logic high	Vref + 0.160	Note2	Vref + 0.160	Note2	-	-	V	1,2,5
VIL.CA(AC160)	AC input logic low	Note2	Vref - 0.160	Note2	Vref - 0.160	-	-	V	1,2,5
VIH.CA(AC135)	AC Input logic high	Vref + 0.135	Note2	Vref + 0.135	Note2	Vref + 0.135	Note2	V	1,2,5
VIL.CA(AC135)	AC input logic low	Note2	Vref - 0.135	Note2	Vref - 0.135	Note2	Vref - 0.135	V	1,2,5
VIH.CA(AC125)	AC Input logic high	-	-	-	-	Vref + 0.125	Note2	V	1,2,5
VIL.CA(AC125)	AC input logic low	-	-	-	-	Note2	Vref - 0.125	V	1,2,5
$V_{RefCA(DC)}$	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	3,4

Notes:

1. For input only pins except $\overline{\text{RESET}}$, Vref = VrefCA (DC).
2. Refer to "Overshoot and Undershoot Specifications" on page 27.
3. The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{RefCA(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 13.5 mV).
4. For reference: approx. VDD/2 +/- 13.5 mV
5. These levels apply for 1.35 volt (see table above) operation only. If the device is operated at 1.5V (table "Single Ended AC and DC Input Levels for DQ and DM" on page 15), the respective levels in JESD79-3 (VIH/L.CA(DC100), VIH/L.CA(AC175), VIH/L.CA(AC150), VIH/L.CA(AC135), VIH/L.CA(AC125) etc.) apply. The 1.5V levels (VIH/L.CA(DC100), VIH/L.CA(AC175), VIH/L.CA(AC150), VIH/L.CA(AC135), VIH/L.CA(AC125) etc.) do not apply when the device is operated in the 1.35 voltage range.

AC and DC Input Levels for Single-Ended Signals

DDR3 SDRAM will support two Vih/Vil AC levels for DDR3-800 and DDR3-1066s specified in table below. DDR3 SDRAM will also support corresponding tDS values (Table 43 and Table 50 in “DDR3L Device Operation”) as well as derating tables Table 46 in “DDR3L Device Operation” depending on Vih/Vil AC levels.

Single Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3L-800/1066		DDR3L-1333/1600		DDR3L-1866		Unit	Notes
		Min	Max	Min	Max	Min	Max		
VIH.DQ(DC90)	DC input logic high	Vref + 0.09	VDD	Vref + 0.09	VDD	Vref + 0.09	VDD	V	1
VIL.DQ(DC90)	DC input logic low	VSS	Vref - 0.09	VSS	Vref - 0.09	VSS	Vref - 0.09	V	1
VIH.DQ(AC160)	AC input logic high	Vref + 0.160	Note2	-	-	-	-	V	1, 2, 5
VIL.DQ(AC160)	AC input logic low	Note2	Vref - 0.160	-	-	-	-	V	1, 2, 5
VIH.DQ(AC135)	AC Input logic high	Vref + 0.135	Note2	Vref + 0.135	Note2	-	-	V	1, 2, 5
VIL.DQ(AC135)	AC input logic low	Note2	Vref - 0.135	Note2	Vref - 0.135	-	-	V	1, 2, 5
VIH.DQ(AC130)	AC Input logic high	-	-	-	-	Vref + 0.130	Note2	V	1, 2, 5
VIL.DQ(AC130)	AC input logic low	-	-	-	-	Note2	Vref - 0.130	V	1, 2, 5
$V_{RefDQ(DC)}$	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V	3, 4

Notes:

1. Vref = VrefDQ (DC).
2. Refer to "Overshoot and Undershoot Specifications" on page 27.
3. The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{RefDQ(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 13.5 mV). 4. For reference: approx. VDD/2 +/- 13.5 mV
4. For reference: approx. VDD/2 +/- 13.5 mV
5. These levels apply for 1.35 volt (table "Single Ended AC and DC Input Levels for Command and Address" on page 14) operation only. If the device is operated at 1.5V (table above), the respective levels in JESD79-3 (VIH/L.DQ(DC100), VIH/L.DQ(AC175), VIH/L.DQ(AC150), VIH/L.DQ(AC135) etc.) apply. The 1.5V levels (VIH/L.DQ(DC100), VIH/L.DQ(AC175), VIH/L.DQ(AC150), VIH/L.DQ(AC135) etc.) do not apply when the device is operated in the 1.35 voltage range.

Vref Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages $_{VRefCA}$ and V_{RefDQ} are illustrated in figure below. It shows a valid reference voltage V_{Ref} (t) as a function of time. (V_{Ref} stands for V_{RefCA} and V_{RefDQ} likewise).

V_{Ref} (DC) is the linear average of V_{Ref} (t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in the table "Differential Input Slew Rate Definition" on page 22. Furthermore V_{Ref} (t) may temporarily deviate from $V_{Ref\ (DC)}$ by no more than +/- 1% VDD.

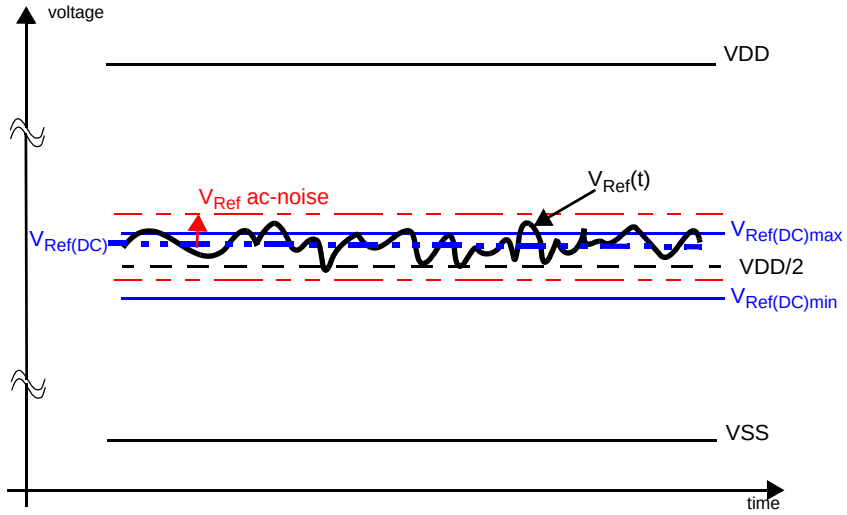


Illustration of $V_{Ref(DC)}$ tolerance and V_{Ref} ac-noise limits

The voltage levels for setup and hold time measurements $V_{IH(AC)}$, $V_{IH(DC)}$, $V_{IL(AC)}$, and $V_{IL(DC)}$ are dependent on V_{Ref}.

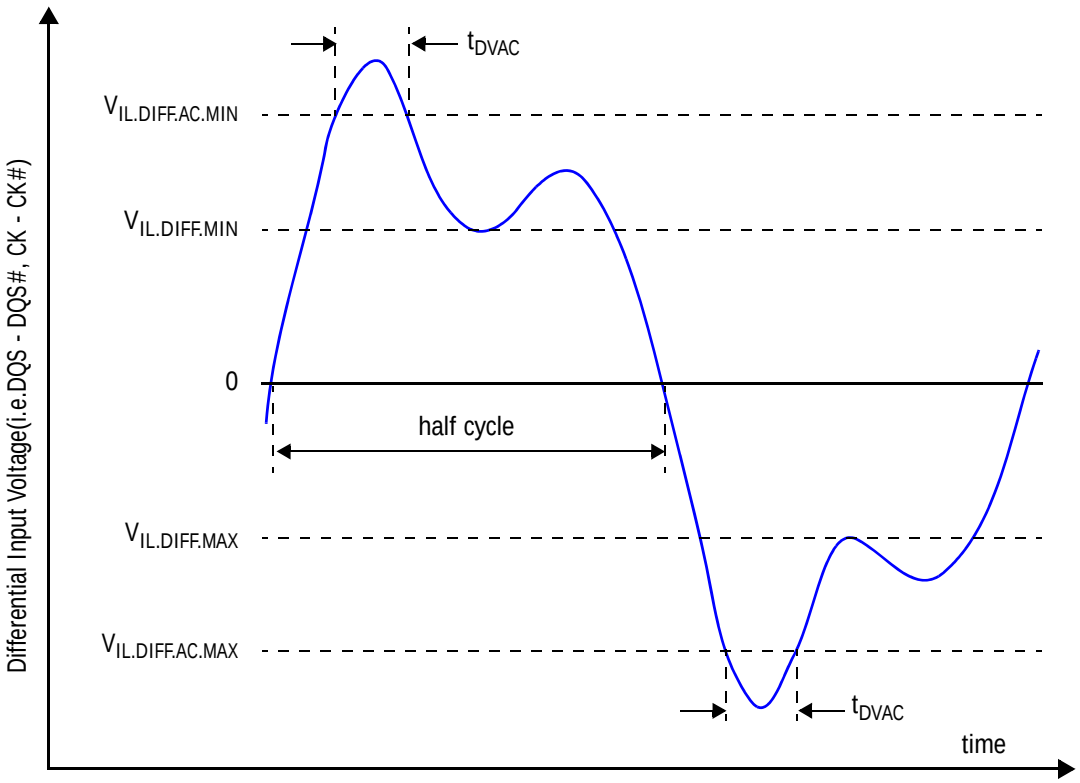
"V_{Ref}" shall be understood as $V_{Ref(DC)}$, as defined in figure above.

This clarifies that dc-variations of V_{Ref} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{Ref(DC)}$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{Ref}ac-noise. Timing and voltage effects due to ac-noise on V_{Ref} up to the specified limit (+/- 1% of VDD) are included in DRAM timings and their associated deratings.

AC and DC Logic Input Levels for Differential Signals

Differential signal definition



Definition of differential ac-swing and "time above ac-level" t_{DVAC}

Differential swing requirements for clock (CK - $\overline{CK}$) and strobe (DQS-$\overline{DQS}$)

Differential AC and DC Input Levels

Symbol	Parameter	DDR3L-800, 1066, 1333, 1600, 1866		Unit	Notes
		Min	Max		
V_{IHdiff}	Differential input high	+ 0.180	Note 3	V	1
V_{ILdiff}	Differential input logic low	Note 3	- 0.180	V	1
$V_{IHdiff\ (ac)}$	Differential input high ac	2 x (VIH (ac) - Vref)	Note 3	V	2
$V_{ILdiff\ (ac)}$	Differential input low ac	Note 3	2 x (VIL (ac) - Vref)	V	2

Notes:

1. Used to define a differential signal slew-rate.
2. For CK - $\overline{CK}$ use VIH/VIL (ac) of AADD/CMD and VREFCA; for DQS - $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ use VIH/VIL (ac) of DQs and VREFDQ; if a reduced ac-high or ac-low levels is used for a signal group, then the reduced level applies also here.
3. These values are not defined; however, the single-ended signals Ck, $\overline{CK}$, DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ need to be within the respective limits (VIH (dc) max, VIL (dc) min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" on page 27.

Allowed time before ringback (tDVAC) for CK - $\overline{CK}$ and DQS - $\overline{DQS}$

Slew Rate [V/ns]	DDR3L-800/1066/1333/1600				DDR3L-1866					
	tDVAC [ps] @ |VIH/Ldiff (ac)| = 320mV		tDVAC [ps] @ |VIH/Ldiff (ac)| = 270mV		tDVAC [ps] @ |VIH/Ldiff (ac)| = 270mV		tDVAC [ps] @ |VIH/Ldiff (ac)| = 250mV		tDVAC [ps] @ |VIH/Ldiff (ac)| = 260mV	
	min	max	min	max	min	max	min	max	min	max
> 4.0	189	-	201	-	163	-	168	-	176	-
4.0	189	-	201	-	163	-	168	-	176	-
3.0	162	-	179	-	140	-	147	-	154	-
2.0	109	-	134		95		105		111	
1.8	91	-	119	-	80	-	91	-	97	-
1.6	69	-	100	-	62	-	74	-	78	-
1.4	40	-	76	-	37	-	52	-	56	-
1.2	note	-	44	-	5	-	22	-	24	-
1.0	note	-	note	-	note	-	note	-	note	-
< 1.0	note	-	note	-	note	-	note	-	note	-

note : Rising input signal shall become equal to or greater than VIH(ac) level and Falling input signal shall become equal to or less than VIL(ac) level.

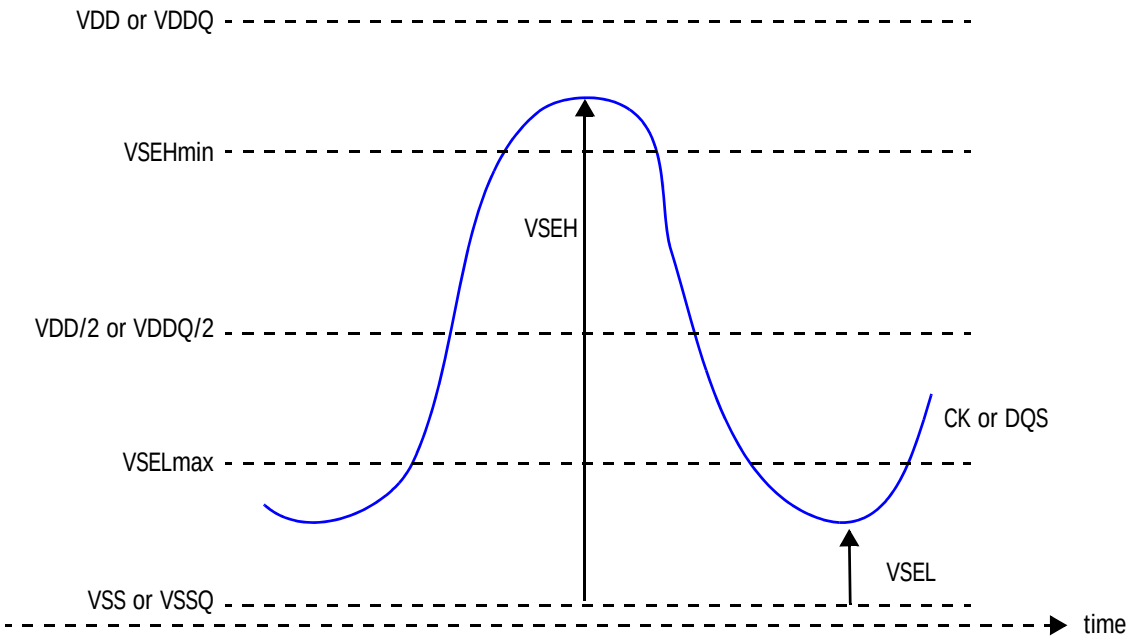
Single-ended requirements for differential signals

Each individual component of a differential signal (CK, DQS, DQSL, DQSU, $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$, of $\overline{DQSU}$) has also to comply with certain requirements for single-ended signals.

CK and CK have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH (ac) / VIL (ac)) for ADD/CMD signals) in every half-cycle.

DQS, DQSL, DQSU, $\overline{DQS}$, $\overline{DQSL}$ have to reach VSEHmin / VSELmax (approximately the ac-levels (VIH (ac) / VIL (ac)) for DQ signals) in every half-cycle preceding and following a valid transition.

Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g., if VIH.CA(AC150)/VIL.CA(AC150) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and $\overline{CK}$.



Single-ended requirements for differential signals.

Note that, while ADD/CMD and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. the transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Single-ended levels for CK, DQS, DQSL, DQSU, $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$ or $\overline{DQSU}$

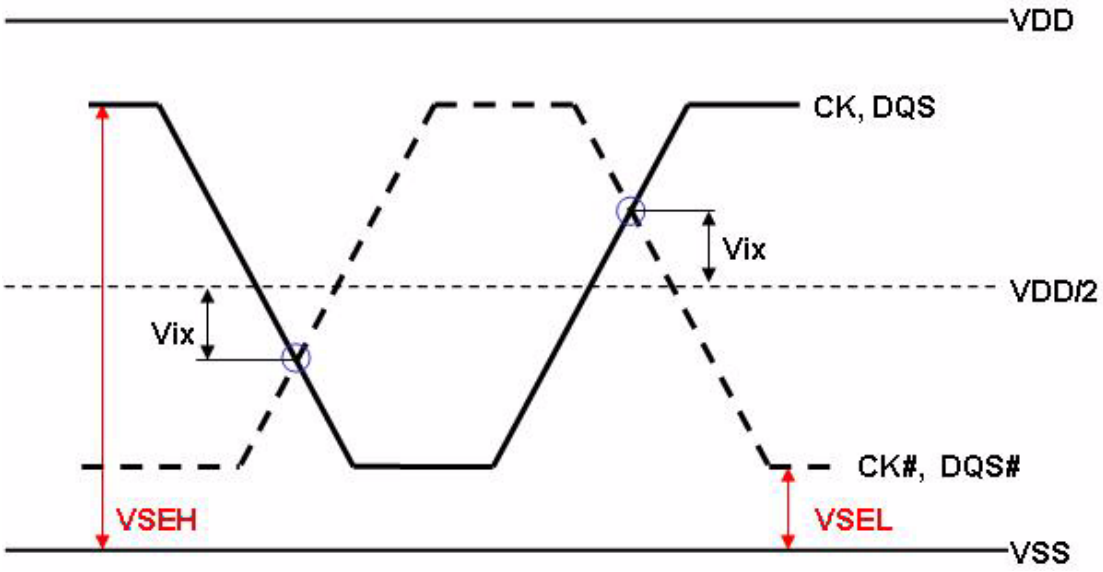
Symbol	Parameter	DDR3L-800, 1066, 1333, 1600, 1866		Unit	Notes
		Min	Max		
VSEH	Single-ended high level for strobes	(VDD / 2) + 0.175	Note 3	V	1,2
	Single-ended high level for Ck, $\overline{CK}$	(VDD /2) + 0.175	Note 3	V	1,2
VSEL	Single-ended low level for strobes	Note 3	(VDD / 2) - 0.175	V	1,2
	Single-ended low level for CK, $\overline{CK}$	Note 3	(VDD / 2) - 0.175	V	1,2

Notes:

1. For CK, $\overline{CK}$ use VIH/VIL (ac) of ADD/CMD; for strobes (DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$) use VIH/VIL (ac) of DQs.
2. VIH (ac)/VIL (ac) for DQs is based on VREFDQ; VIH (ac)/VIL (ac) for ADD/CMD is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined; however, the single-ended signals Ck, $\overline{CK}$, DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ need to be within the respective limits (VIH (dc) max, VIL (dc) min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications" on page 27.

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must meet the requirements in table below. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS



Vix Definition

Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	DDR3L-800, 1066, 1333, 1600, 1866		Unit	Notes
		Min	Max		
V_{IX}(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK, $\overline{CK}$	-150	150	mV	2
		-175	175	mV	1
V_{IX}(DQS)	Differential Input Cross Point Voltage relative to VDD/2 for DQS, $\overline{DQS}$	-150	150	mV	2

Notes:

1. Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and $\overline{CK}$ are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/-250 mV, and when the differential slew rate of CK - $\overline{CK}$ is larger than 3 V/ns.
2. The relation between Vix Min/Max and VSEL/VSEH should satisfy following.
   (VDD/2) + Vix (Min) - VSEL $\geq$ 25mV
   VSEH - ((VDD/2) + Vix (Max)) $\geq$ 25mV

Slew Rate Definitions for Single-Ended Input Signals

See 7.5 “Address / Command Setup, Hold and Derating” in “DDR3L Device Operation” for single-ended slew rate definitions for address and command signals.

See 7.6 “Data Setup, Hold and Slew Rate Derating” in “DDR3L Device Operation” for single-ended slew rate definition for data signals.

Slew Rate Definitions for Differential Input Signals

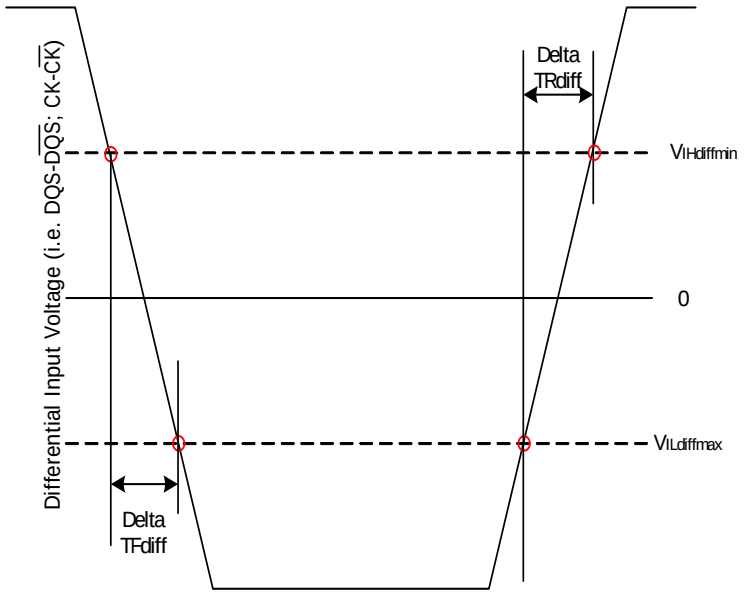
Input slew rate for differential signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) are defined and measured as shown in table and figure below.

Differential Input Slew Rate Definition

Description	Measured		Defined by
	Min	Max	
Differential input slew rate for rising edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin}-V_{ILdiffmax}]$ / DeltaTRdiff
Differential input slew rate for falling edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin}-V_{ILdiffmax}]$ / DeltaTFdiff

Notes:

The differential signal (i.e. CK-$\overline{CK}$ and DQS-$\overline{DQS}$) must be linear between these thresholds.



Differential Input Slew Rate Definition for DQS, $\overline{DQS}$ and CK, $\overline{CK}$

AC & DC Output Measurement Levels

Single Ended AC and DC Output Levels

Table below shows the output levels used for measurements of single ended signals.

Single-ended AC and DC Output Levels

Symbol	Parameter	DDR3L-800, 1066, 1333, 1600, 1866	Unit	Notes
$V_{OH(DC)}$	DC output high measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
$V_{OM(DC)}$	DC output mid measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
$V_{OL(DC)}$	DC output low measurement level (for IV curve linearity)	0.2 x V_{DDQ}	V	
$V_{OH(AC)}$	AC output high measurement level (for output SR)	V_{TT} + 0.1 x V_{DDQ}	V	1
$V_{OL(AC)}$	AC output low measurement level (for output SR)	V_{TT} - 0.1 x V_{DDQ}	V	1

Notes:

1. The swing of ± 0.1 x V_{DDQ} is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to V_{TT} = V_{DDQ} / 2.

Differential AC and DC Output Levels

Table below shows the output levels used for measurements of single ended signals.

Differential AC and DC Output Levels

Symbol	Parameter	DDR3L-800, 1066, 1333, 1600, 1866	Unit	Notes
$V_{OHdiff\ (AC)}$	AC differential output high measurement level (for output SR)	+ 0.2 x V_{DDQ}	V	1
$V_{OLdiff\ (AC)}$	AC differential output low measurement level (for output SR)	- 0.2 x V_{DDQ}	V	1

Notes:

1. The swing of ± 0.2 x V_{DDQ} is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to V_{TT} = V_{DDQ}/2 at each of the differential outputs.

Single Ended Output Slew Rate

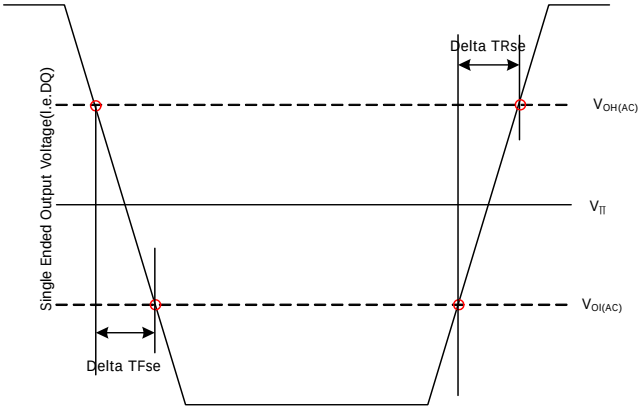
When the Reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals are shown in table and Figure below.

Single-ended Output slew Rate Definition

Description	Measured		Defined by
	From	To	
Single-ended output slew rate for rising edge	$V_{OL(AC)}$	$V_{OH(AC)}$	[$V_{OH(AC)}$-$V_{OL(AC)}$] / DeltaTRse
Single-ended output slew rate for falling edge	$V_{OH(AC)}$	$V_{OL(AC)}$	[$V_{OH(AC)}$-$V_{OL(AC)}$] / DeltaTFse

Notes:

1. Output slew rate is verified by design and characterisation, and may not be subject to production test.



Single Ended Output slew Rate Definition

Output Slew Rate (single-ended)

		DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single-ended Output Slew Rate	SRQse	1.75	5[1)]	1.75	5[1)]	1.75	5[1)]	1.75	5[1)]	1.75	5[1)]	V/ns

Description: SR; Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

se: Single-ended Signals

For Ron = RZQ/7 setting

Note 1): In two cases, a maximum slew rate of 6V/ns applies for a single DQ signal within a byte lane.

Case 1 is a defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).

Case 2 is a defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane switching into the opposite direction (i.e. from low to high of high to low respectively). For the remaining DQ signal switching in to the opposite direction, the regular maximum limite of 5 V/ns applies.

Differential Output Slew Rate

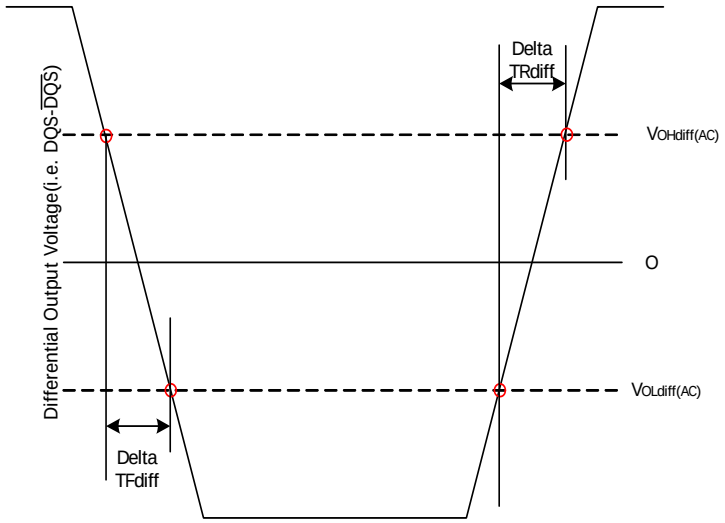
With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff (AC) and VOHdiff (AC) for differential signals as shown in table and figure below.

Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff\ (AC)}$	$V_{OHdiff\ (AC)}$	$[V_{OHdiff\ (AC)}-V_{OLdiff\ (AC)}]$ / DeltaTRdiff
Differential output slew rate for falling edge	$V_{OHdiff\ (AC)}$	$V_{OLdiff\ (AC)}$	$[V_{OHdiff\ (AC)}-V_{OLdiff\ (AC)}]$ / DeltaTFdiff

Notes:

1. Output slew rate is verified by design and characterization, and may not be subject to production test.



Differential Output slew Rate Definition

Differential Output Slew Rate

Parameter	Symbol	DDR3L-800		DDR3L-1066		DDR3L-1333		DDR3L-1600		DDR3L-1866		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential Output Slew Rate	SRQdiff	3.5	12	3.5	12	3.5	12	3.5	12	3.5	12	V/ns

Description: SR; Slew Rate

Q: Query Output (like in DQ, which stands for Data-in, Query-Output)

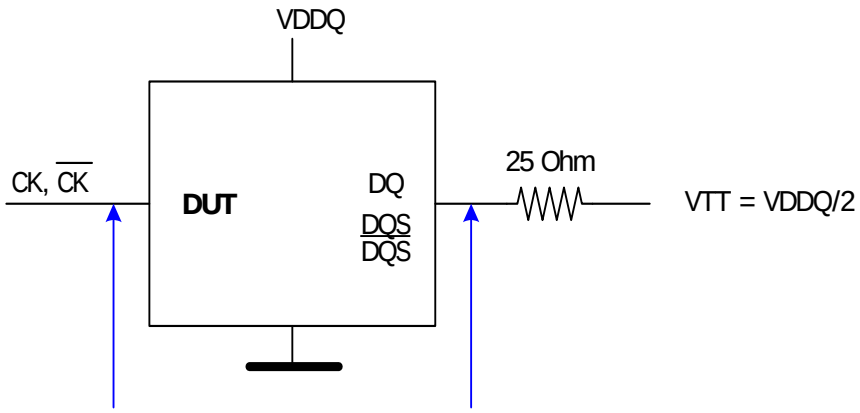
se: Single-ended Signals

For Ron = RZQ/7 setting

Reference Load for AC Timing and Output Slew Rate

Figure below represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



Reference Load for AC Timing and Output Slew Rate

Overshoot and Undershoot Specifications

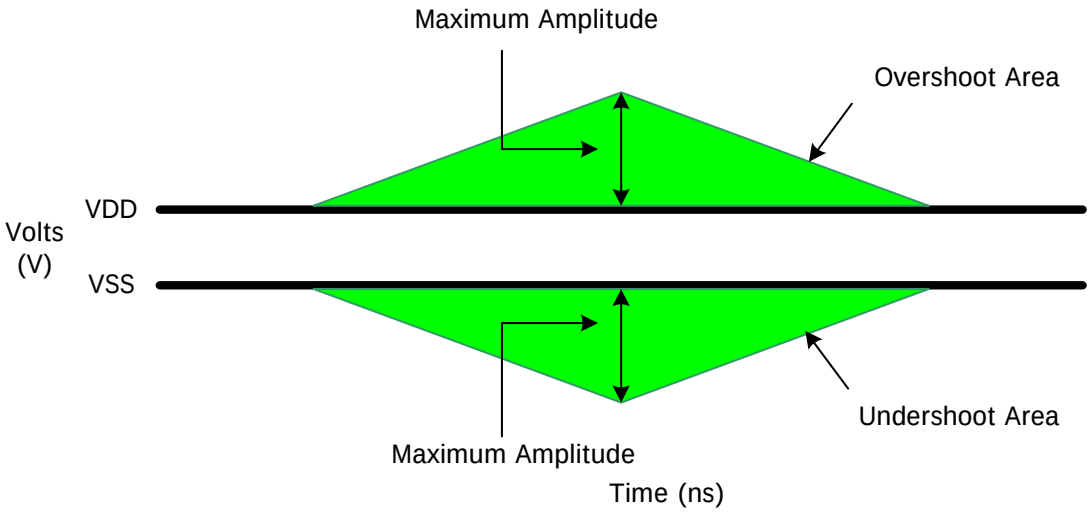
Address and Control Overshoot and Undershoot Specifications

AC Overshoot/Undershoot Specification for Address and Control Pins

Parameter	DDR3 L-800	DDR3 L-1066	DDR3 L-1333	DDR3 L-1600	DDR3 L-1866	Units
Maximum peak amplitude allowed for overshoot area. (See Figure below)	0.4	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area. (See Figure below)	0.4	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDD (See Figure below)	0.67	0.5	0.4	0.33	0.28	V-ns
Maximum undershoot area below VSS (See Figure below)	0.67	0.5	0.4	0.33	0.28	V-ns

(A0-A15, BA0-BA3, CS, RAS, CAS, WE, CKE, ODT)

See figure below for each parameter definition



Address and Control Overshoot and Undershoot Definition

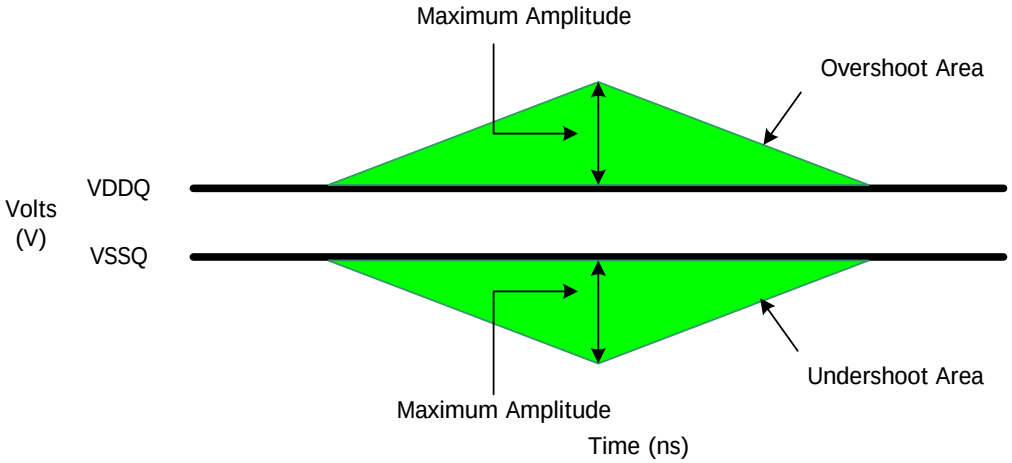
Clock, Data, Strobe and Mask Overshoot and Undershoot Specifications

AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask

Parameter	DDR3 L-800	DDR3 L-1066	DDR3 L-1333	DDR3 L-1600	DDR3 L-1866	Units
Maximum peak amplitude allowed for overshoot area. (See Figure below)	0.4	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area. (See Figure below)	0.4	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDD (See Figure below)	0.25	0.19	0.15	0.13	0.11	V-ns
Maximum undershoot area below VSS (See Figure below)	0.25	0.19	0.15	0.13	0.11	V-ns

(CK, $\overline{CK}$, DQ, DQS, $\overline{DQS}$, DM)

See figure below for each parameter definition



Clock, Data, Strobe and Mask Overshoot and Undershoot Definition

Refresh parameters by device density

Refresh parameters by device density

Parameter	RTT_Nom Setting		512Mb	1Gb	2Gb	4Gb	8Gb	Units
REF command ACT or REF command time	tRFC		90	110	160	260	350	ns
Average periodic refresh interval	tREFI	0 °C ≤ T_{CASE} ≤ 85 °C	7.8	7.8	7.8	7.8	7.8	us
		85 °C < T_{CASE} ≤ 95 °C	3.9	3.9	3.9	3.9	3.9	us

Notes:

1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this materia.

Standard Speed Bins

DDR3 SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

DDR3L-800 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 35.

Speed Bin			DDR3L-800E		Unit	Notes
CL - nRCD - nRP			6-6-6			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	15	20	ns	
ACT to internal read or write delay time		t_{RCD}	15	—	ns	
PRE command period		t_{RP}	15	—	ns	
ACT to ACT or REF command period		t_{RC}	52.5	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	3.0	3.3	ns	1,2,3,4,9,10
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3
Supported CL Settings			5, 6		n_{CK}	10
Supported CWL Settings			5		n_{CK}	

DDR3L-1066 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 35.

Speed Bin			DDR3L-1066F		Unit	Note
CL - nRCD - nRP			7-7-7			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.125	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.125	—	ns	
PRE command period		t_{RP}	13.125	—	ns	
ACT to ACT or REF command period		t_{RC}	50.625	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	3.0	3.3	ns	1,2,3,4,6,9,10
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,6
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3
Supported CL Settings			5, 6, 7, 8		n_{CK}	10
Supported CWL Settings			5, 6		n_{CK}	

DDR3L-1333 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 35.

Speed Bin			DDR3L-1333H		Unit	Note
CL - nRCD - nRP			9-9-9			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.5 (13.125)[5,8]	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.5 (13.125)[5,8]	—	ns	
PRE command period		t_{RP}	13.5 (13.125)[5,8]	—	ns	
ACT to ACT or REF command period		t_{RC}	49.5 (49.125)[5,8]	—	ns	
ACT to PRE command period		t_{RAS}	36	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	3.0	3.3	ns	1,2,3,4,7,9,10
	CWL = 6, 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,7
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,4,7
			(Optional)[5,8]			
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3,4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3
			(Optional)		ns	5
Supported CL Settings			5, 6, 7, 8, 9, 10		n_{CK}	
Supported CWL Settings			5, 6, 7		n_{CK}	

DDR3L-1600 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 35.

Speed Bin			DDR3L-1600K		Unit	Note
CL - nRCD - nRP			11-11-11			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.75 (13.125)[5,9]	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.75 (13.125)[5,9]	—	ns	
PRE command period		t_{RP}	13.75 (13.125)[5,9]	—	ns	
ACT to ACT or REF command period		t_{RC}	48.75 (48.125)[5,9]	—	ns	
ACT to PRE command period		t_{RAS}	35	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	3.0	3.3	ns	1,2,3,4,8,10,11
	CWL = 6, 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,8
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,4,8
			(Optional)[5,9]			
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,8
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3,4,8
			(Optional)[5,9]			
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 11	CWL = 5, 6,7	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	<1.5	ns	1,2,3
Supported CL Settings			5, 6, 7, 8, 9, 10, 11		n_{CK}	
Supported CWL Settings			5, 6, 7, 8		n_{CK}	

DDR3L-1866 Speed Bins

For specific Notes See "Speed Bin Table Notes" on page 35.

Speed Bin			DDR3L-1866M		Unit	Note
CL - nRCD - nRP			13-13-13			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.91 (13.125)[5,12]	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.91 (13.125)[5,12]	—	ns	
PRE command period		t_{RP}	13.91 (13.125)[5,12]	—	ns	
ACT to PRE command period		t_{RAS}	34	9 * tREFI	ns	
ACT to ACT or PRE command period		t_{RC}	47.91 (47.125)[5,12]	-	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	3.0	3.3	ns	1, 2, 3, 4, 9
	CWL = 6,7,8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1, 2, 3, 9
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 9
	CWL = 7,8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1, 2, 3, 4, 9
			(Optinal)			
	CWL = 7,8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1, 2, 3, 9
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 9
	CWL = 8,9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1, 2, 3, 4, 9
			(Optinal)			
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 9
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1, 2, 3, 9
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4, 9
CL = 11	CWL = 5,6,7	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	<1.5	ns	1, 2, 3, 4, 9
			(Optinal)			
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	1, 2, 3, 4
CL = 12	CWL = 5,6,7,8	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 13	CWL = 5,6,7,8	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	1.07	<1.25	ns	1, 2, 3
Supported CL Settings			6, 7, 8, 9, 10, 11,13		n_{CK}	
Supported CWL Settings			5, 6, 7, 8, 9		n_{CK}	

Speed Bin Table Notes

Absolute Specification (T_{OPER}; V_{DDQ} = V_{DD} = 1.35V +0.100/- 0.067 V);

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (3.0, 2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next 'Supported CL', where tCK(AVG) = 3.0 ns should only be used for CL = 5 calculation.
3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to DIMM data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
10. DDR3 SDRAM devices supporting optional down binning to CL=7 and CL=9, and tAA/tRCD/tRP must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3-1333H devices supporting down binning to DDR3-1066F should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600K devices supporting down binning to DDR3-1333H or DDR3-1600F should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accordingly. For example, 49.125ns (tRASmin + tRPmin = 36 ns + 13.125 ns) for DDR3-1333H and 48.125ns (tRASmin + tRPmin = 35 ns + 13.125 ns) for DDR3-1600K.
11. For CL5 support, refer to DIMM SPD information. DRAM is required to support CL5. CL5 is not mandatory in SPD coding.
12. DDR3 SDRAM devices supporting optional down binning to CL=11, CL=9 and CL=7, tAA/tRCD/tRPmin must be 13.125ns. SPD setting must be programed to match. For example, DDR3-1866M devices supporting down binning to DDR3-1600K or DDR3-1333H or 1066F should program 13.125ns in SPD bytes for tAAmin(byte16), tRCDmin(byte18) and tRPmin(byte20). Once tRP (byte20) is programmed to 13.125ns, tRCmin(byte 21,23) also should be programmed accordingly. For example, 47.125ns(tRASmin + tRPmin = 34ns + 13.125ns)

Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating temperature	0 to 65	^{o}C	1, 3
H_{OPR}	Operating humidity (relative)	10 to 90	%	1
T_{STG}	Storage temperature	-50 to +100	^{o}C	1
H_{STG}	Storage humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1, 2

Note:

1. Stress greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Expousure to absolute maximum rating conditions for extended periods may affect reliablility.
2. Up to 9850 ft.
3. The designer must meet the case temperature specifications for individual module components.

IDD and IDDQ Specification Parameters and Test Conditions

IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined. Figure 1. shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
  Attention: IDDQ values cannot be directly used to calculate IO power of the DDR3 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 2. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply:

- ”0” and “LOW” is defined as VIN <= $V_{ILAC(max)}$.
- ”1” and “HIGH” is defined as VIN >= $V_{IHAC(max)}$.
- “MID_LEVEL” is defined as inputs are VREF = VDD/2.
- Timing used for IDD and IDDQ Measurement-Loop Patterns are provided in Table 1.
- Basic IDD and IDDQ Measurement Conditions are described in Table 2.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 3 through Table 10.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting
  RON = RZQ/7 (34 Ohm in MR1);
  Qoff = 0_B (Output Buffer enabled in MR1);
  RTT_Nom = RZQ/6 (40 Ohm in MR1);
  RTT_Wr = RZQ/2 (120 Ohm in MR2);
  TDQS Feature disabled in MR1
- Attention: The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, LOW, LOW, LOW}
- Define $\overline{D}$ = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, HIGH, HIGH, HIGH}

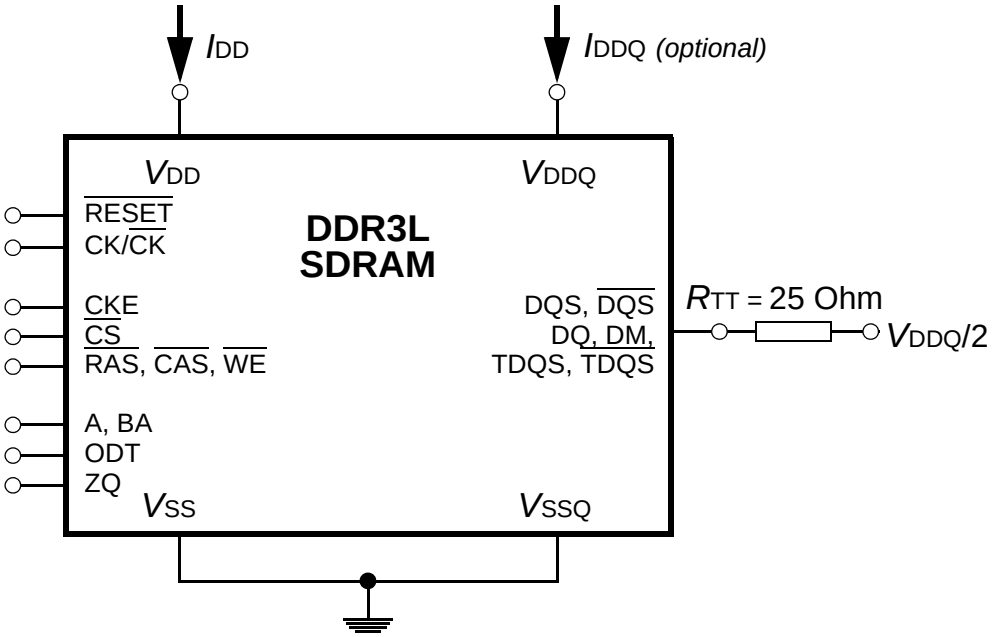


Figure 1 - Measurement Setup and Test Load for IDD and IDDQ (optional) Measurements
[Note: DIMM level Output test load condition may be different from above

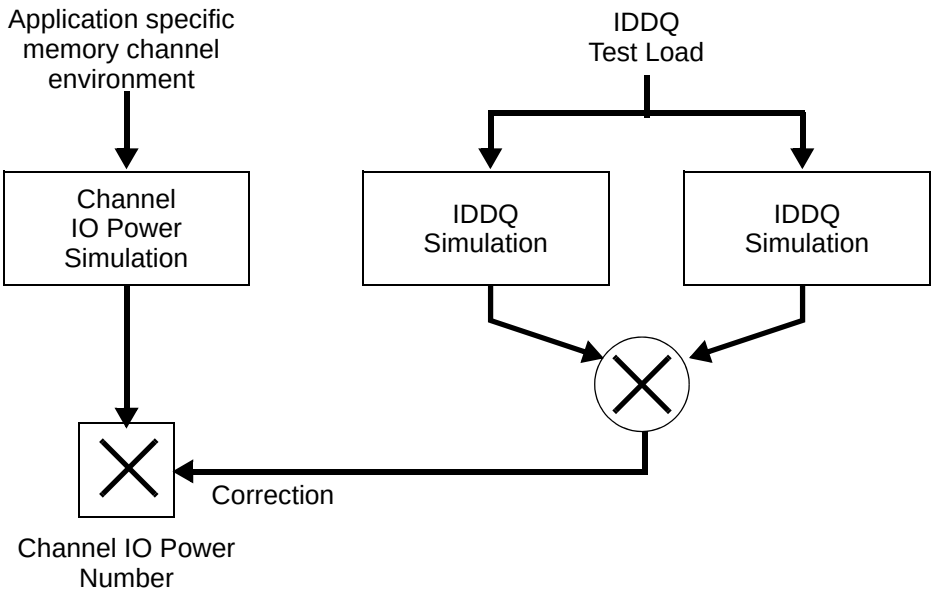


Figure 2 - Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement

Table 1 -Timings used for IDD and IDDQ Measurement-Loop Patterns

Symbol		DDR3L-1066	DDR3L-1333	DDR3L-1600	DDR3L-1866	Unit
		7-7-7	9-9-9	11-11-11	13-13-13	
t_{CK}		1.875	1.5	1.25	1.07	ns
CL		7	9	11	13	nCK
n_{RCD}		7	9	11	13	nCK
n_{RC}		27	33	39	45	nCK
n_{RAS}		20	24	28	32	nCK
n_{RP}		7	9	11	13	nCK
n_{FAW}	1KB page size	20	20	24	26	nCK
	2KB page size	27	30	32	33	nCK
n_{RRD}	1KB page size	4	4	5	5	nCK
	2KB page size	6	5	6	6	nCK
n_{RFC} -512Mb		48	60	72	85	nCK
n_{RFC}-1 Gb		59	74	88	103	nCK
n_{RFC}- 2 Gb		86	107	128	150	nCK
n_{RFC}- 4 Gb		139	174	208	243	nCK
n_{RFC}- 8 Gb		187	234	280	328	nCK

Table 2 -Basic IDD and IDDQ Measurement Conditions

Symbol	Description
I_{DD0}	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling according to Table 3; Data IO: MID-LEVEL; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 3); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 3.
I_{DD1}	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: High between ACT, RD and PRE; Command, Address; Bank Address Inputs, Data IO: partially toggling according to Table 4; DM: stable at 0; Bank Activity: Cycling with on bank active at a time: 0,0,1,1,2,2,... (see Table 4); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 4.

Symbol	Description
I_{DD2N}	Precharge Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 5.
I_{DD2NT}	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 6; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: toggling according to Table 6; Pattern Details: see Table 6.
I_{DD2P0}	Precharge Power-Down Current Slow Exit CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit[c]
I_{DD2P1}	Precharge Power-Down Current Fast Exit CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit[c]
I_{DD2Q}	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0
I_{DD3N}	Active Standby Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 5.
I_{DD3P}	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 1; BL: 8[a]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0

Symbol	Description
I_{DD4R}	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: High between RD; Command, Address, Bank Address Inputs: partially toggling according to Table 7; Data IO: seamless read data burst with different data between one burst and the next one according to Table 7; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...(see Table 7); Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 7.
I_{DD4W}	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: High between WR; Command, Address, Bank Address Inputs: partially toggling according to Table 8; Data IO: seamless read data burst with different data between one burst and the next one according to Table 8; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...(see Table 8); Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at HIGH; Pattern Details: see Table 8.
I_{DD5B}	Burst Refresh Current CKE: High; External clock: On; tCK, CL, nRFC: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$: High between REF; Command, Address, Bank Address Inputs: partially toggling according to Table 9; Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: REF command every nREF (see Table 9); Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 9.
I_{DD6}	Self-Refresh Current: Normal Temperature Range T_{CASE}: 0 - 85 °C; Auto Self-Refresh (ASR): Disabled[d)];Self-Refresh Temperature Range (SRT): Normal[e)]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: MID_LEVEL
I_{DD6ET}	Self-Refresh Current: Extended Temperature Range T_{CASE}: 0 - 95 °C; Auto Self-Refresh (ASR): Disabled[d)];Self-Refresh Temperature Range (SRT): Extended[e)]; CKE: Low; External clock: Off; CK and $\overline{CK}$: LOW; CL: see Table 1; BL: 8[a)]; AL: 0; $\overline{CS}$, Command, Address, Bank Address Inputs, Data IO: MID_LEVEL; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: MID_LEVEL

Symbol	Description
I_{DD7}	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, NRRD, nFAW, CL: see Table 1; BL: 8[a,f]; AL: CL-1; $\overline{CS}$: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling according to Table 10; Data IO: read data burst with different data between one burst and the next one according to Table 10; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1,...7) with different addressing, wee Table 10; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 10.

a) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B

b) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B

c) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12 = 1B for Fast Exit

d) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable

e) Self-Refresh Temperature Range (SRT): set MR2 A7 = 0B for normal or 1B for extended temperature range

f) Read Burst Type: Nibble Sequential, set MR0 A[3] = 0B

Table 3 - IDD0 Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1, 2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC+3, 4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern 1...4 until 1*nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern 1...4 until 2*nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.

b) DQ signals are MID-LEVEL.

Table 4 - IDD1 Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRCD - 1, truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1,2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC+3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until nRC + nRCE - 1, truncate if necessary												
			1*nRC+nRCD	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			...	repeat pattern nRC + 1,...4 until nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until *2 nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID_LEVEL.

Table 5 - IDD2N and IDD3N Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
			3	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	8-11	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	12-15	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	16-19	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	20-23	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	24-17	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	28-31	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.
b) DQ signals are MID-LEVEL.

Table 6 - IDD2NT and IDDQ2NT Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
			3	$\overline{D}$	1	1	1	1	0	0	0	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 1												
		2	8-11	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 2												
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 3												
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 4												
		5	20-23	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 5												
		6	24-17	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 6												
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.
b) DQ signals are MID-LEVEL.

Table 7 - IDD4R and IDDQ4R Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2,3	$\overline{D}$,$\overline{D}$	1	1	1	1	0	0	00	0	0	0	0	-
			4	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	00	0	0	F	0	-
			6,7	$\overline{D}$,$\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.
b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

Table 8 - IDD4W Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	00	0	0	0	0	-
			2,3	$\overline{D}$,$\overline{D}$	1	1	1	1	1	0	00	0	0	0	0	-
			4	WR	0	1	0	0	1	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	00	0	0	F	0	-
			6,7	$\overline{D}$,$\overline{D}$	1	1	1	1	1	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to WR Commands, otherwise MID-LEVEL.
b) Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are MID-LEVEL.

Table 9 - IDD5B Measurement-Loop Pattern[a)]

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	REF	0	0	0	1	0	0	0	0	0	0	0	-
		1	1.2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{D}$, $\overline{D}$	1	1	1	1	0	0	00	0	0	F	0	-
			5...8	repeat cycles 1...4, but BA[2:0] = 1												
			9...12	repeat cycles 1...4, but BA[2:0] = 2												
			13...16	repeat cycles 1...4, but BA[2:0] = 3												
			17...20	repeat cycles 1...4, but BA[2:0] = 4												
			21...24	repeat cycles 1...4, but BA[2:0] = 5												
			25...28	repeat cycles 1...4, but BA[2:0] = 6												
			29...32	repeat cycles 1...4, but BA[2:0] = 7												
		2	33...nRFC-1	repeat Sub-Loop 1, until nRFC - 1. Truncate, if necessary.												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are MID-LEVEL.
b) DQ signals are MID-LEVEL.

Table 10 - IDD7 Measurement-Loop Pattern[a)]

ATTENTION! Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

CK, $\overline{CK}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	00	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	00	0	0	0	0	-
			...	repeat above D Command until nRRD - 1												
		1	nRRD	ACT	0	0	1	1	0	1	00	0	0	F	0	-
			nRRD+1	RDA	0	1	0	1	0	1	00	1	0	F	0	00110011
			nRRD+2	D	1	0	0	0	0	1	00	0	0	F	0	-
			...	repeat above D Command until 2* nRRD - 1												
		2	2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 3												
		4	4*nRRD	D	1	0	0	0	0	3	00	0	0	F	0	-
				Assert and repeat above D Command until nFAW - 1, if necessary												
		5	nFAW	repeat Sub-Loop 0, but BA[2:0] = 4												
		6	nFAW+nRRD	repeat Sub-Loop 1, but BA[2:0] = 5												
		7	nFAW+2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 6												
		8	nFAW+3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 7												
		9	nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	F	0	-
				Assert and repeat above D Command until 2* nFAW - 1, if necessary												
		10	2*nFAW+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			2*nFAW+1	RDA	0	1	0	1	0	0	00	1	0	F	0	00110011
			2&nFAW+2	D	1	0	0	0	0	0	00	0	0	F	0	-
				Repeat above D Command until 2* nFAW + nRRD - 1												
		11	2*nFAW+nRRD	ACT	0	0	1	1	0	1	00	0	0	0	0	-
			2*nFAW+nRRD+1	RDA	0	1	0	1	0	1	00	1	0	0	0	00000000
			2&nFAW+nRRD+2	D	1	0	0	0	0	1	00	0	0	0	0	-
				Repeat above D Command until 2* nFAW + 2* nRRD - 1												
		12	2*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 2												
		13	2*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 3												
		14	2*nFAW+4*nRRD	D	1	0	0	0	0	3	00	0	0	0	0	-
				Assert and repeat above D Command until 3* nFAW - 1, if necessary												
		15	3*nFAW	repeat Sub-Loop 10, but BA[2:0] = 4												
		16	3*nFAW+nRRD	repeat Sub-Loop 11, but BA[2:0] = 5												
		17	3*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 6												
		18	3*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 7												
		19	3*nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	0	0	-
				Assert and repeat above D Command until 4* nFAW - 1, if necessary												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise MID-LEVEL.
b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are MID-LEVEL.

IDD Specifications (Tcase: 0 to 95°C)

* Module IDD values in the datasheet are only a calculation based on the component IDD spec.
The actual measurements may vary according to DQ loading cap.

4GB, 512M x 72 U-DIMM: HMT451A7BFR8A

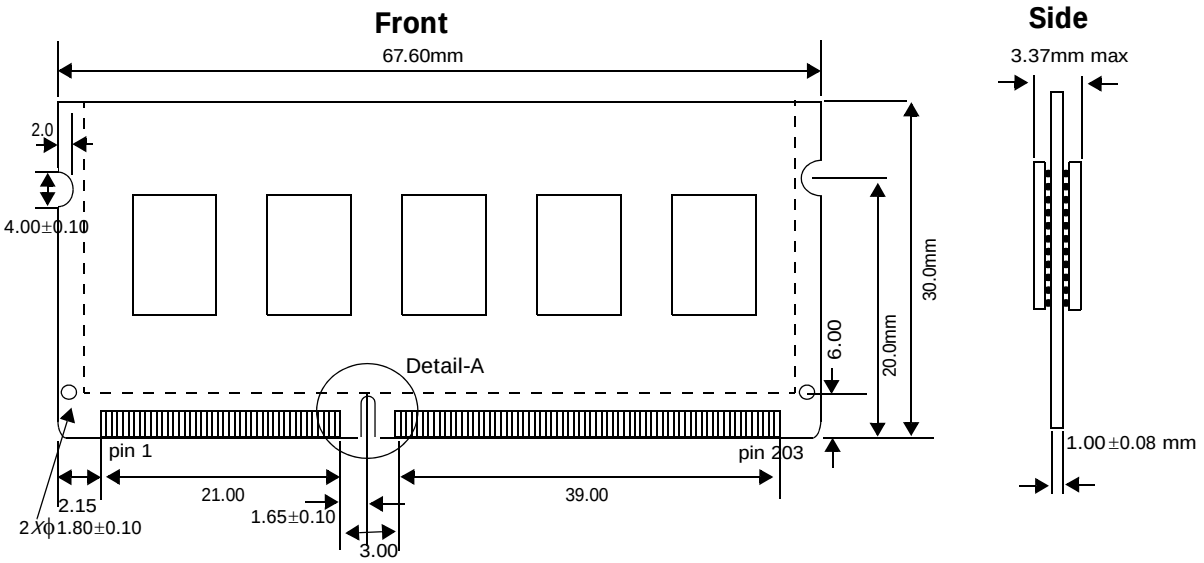
Symbol	DDR3L 1066	DDR3L 1333	DDR3L 1600	DDR3L 1866	Unit	note
IDD0	270	288	297	306	mA	
IDD1	333	351	360	369	mA	
IDD2N	135	144	153	162	mA	
IDD2NT	162	180	189	198	mA	
IDD2P0	72	72	72	72	mA	
IDD2P1	81	90	90	99	mA	
IDD2Q	144	153	153	153	mA	
IDD3N	216	225	234	243	mA	
IDD3P	153	153	162	162	mA	
IDD4R	585	675	765	855	mA	
IDD4W	630	720	810	900	mA	
IDD5B	1800	1800	1800	1800	mA	
IDD6	108	108	108	108	mA	
IDD6ET	144	144	144	144	mA	
IDD7	990	1170	1215	1305	mA	

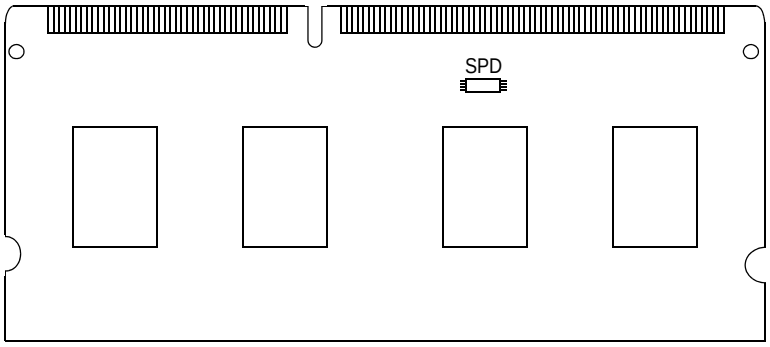
8GB, 1G x 72 U-DIMM: HMT41GA7BFR8A

Symbol	DDR3L 1066	DDR3L 1333	DDR3L 1600	DDR3L 1866	Unit	note
IDD0	405	432	531	549	mA	
IDD1	468	495	594	612	mA	
IDD2N	270	288	306	324	mA	
IDD2NT	324	360	378	396	mA	
IDD2P0	144	144	144	144	mA	
IDD2P1	162	180	180	198	mA	
IDD2Q	288	306	306	306	mA	
IDD3N	432	450	468	486	mA	
IDD3P	306	306	324	324	mA	
IDD4R	720	819	999	1098	mA	
IDD4W	765	864	1044	1143	mA	
IDD5B	1935	1944	2034	2043	mA	
IDD6	216	216	216	216	mA	
IDD6ET	288	288	288	288	mA	
IDD7	1125	1314	1449	1548	mA	

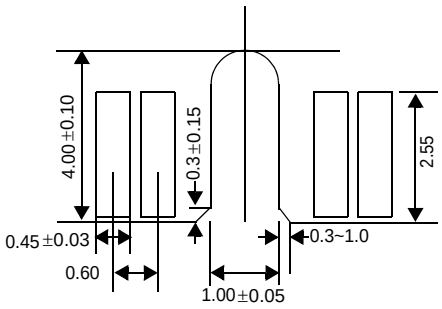
Module Dimensions

512Mx72 - HMT451A7BFR8A





Detail of Contacts A

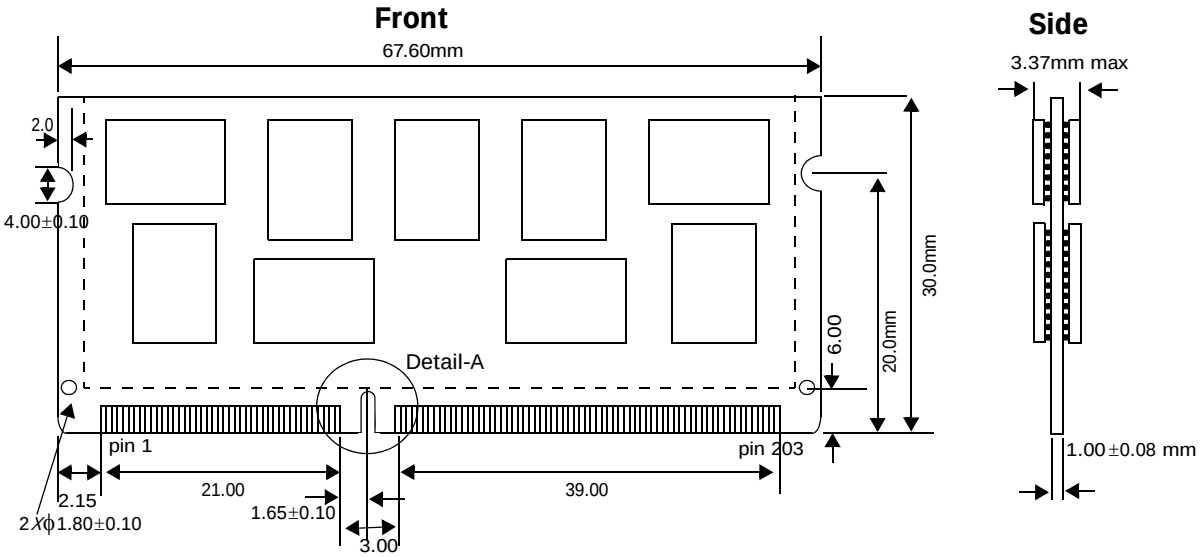


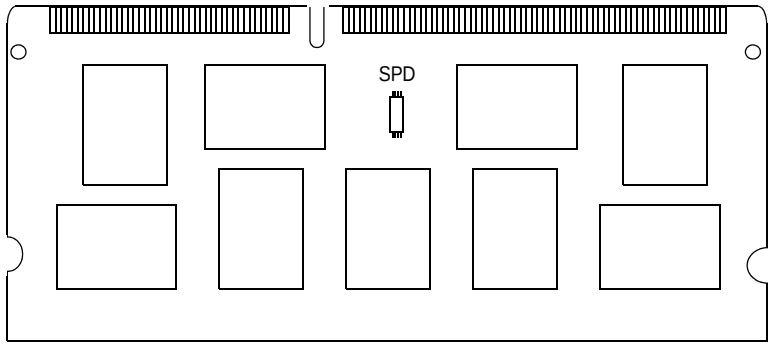
Note:

1. ±0.13 tolerance on all dimensions unless otherwise stated.

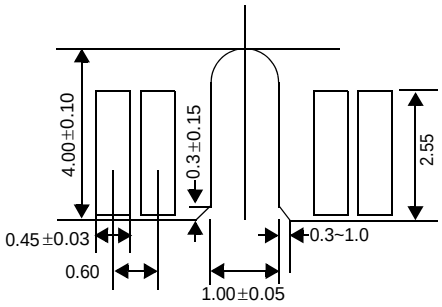
Units: millimeters

1Gx72 - HMT41GA7BFR8A





Detail of Contacts A



Note:

1. ± 0.13 tolerance on all dimensions unless otherwise stated.

Units: millimeters